SIGMATEK

IO 011

S-DIAS Multi I/O Module

Operating Manual

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Translation from German

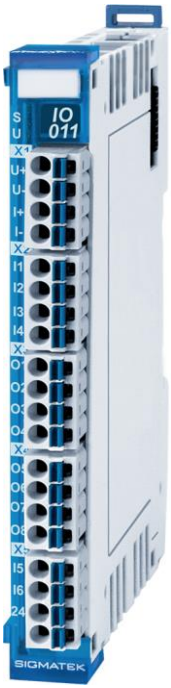
S-DIAS Multi I/O Module IO 011

with 6 digital inputs

8 short-circuit proof digital outputs back-reading

1 analog voltage input

1 analog current input



The module has 6 digital inputs (+24 V/3.5 mA/0.5 ms) and 8 short-circuit proof digital outputs (+24 V/0.5 A), these also support back-reading (0.5 ms).
The voltage supply for the digital outputs are monitored for under voltage.

Additionally, the module has an analog ±10 V input and an analog differential current input (0-20 mA or 4-20 mA).

The resolution of the two analog inputs is 16 bits.

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1 Technical Data

1.1 Digital Input Specifications

Number	6	
Input voltage	typically +24 V	maximum +30 V
Signal level (up to HW version 1.10)	low: < +8 V	high: > +14 V
Signal level (starting with HW version 1.20)	low: < +5 V	high: > +15 V
Input current	3.7 mA at +24 V	
Input delay	typically 0.5 ms	

1.2 Digital Output Specifications

Number	8	
Short-circuit proof	yes	
Maximum permitted continuous load current / channel	0.5 A	
Maximum total current (all 8 outputs)	4 A (100% of on-time)	
Maximum braking energy of outputs (inductive load)	maximum 1 Joule/channel	
Residual current output (off)	≤ 10 µA	
Turn-on delay	< 100 µs	
Turn-off delay	< 150 µs	
Read-back signal level	low: < +8 V	high: > +14 V
Input delay	typically 0.5 ms	
Maximum allowed voltage on the digital output when switched off	A voltage supplied to the digital output pin from external must not exceed the voltage on the supply pin (24 V) by more than 0.7 V.	

1.3 Voltage Monitor

Power supply +24 V	supply voltage > 18 V (DC OK-LED lights green)

1.4 Analog ±10 V Input Specifications

Number of channels	1	
Measurement range	-10 … +10 V	0 ... +10 V
Measurement value	-10,000 ... +10,000 or -30,000 … +30,000 (at full range)	0 ... +10,000 or 0 … +30,000 (at full range)
	With an open input, the firmware returns the positive maximum value and a status bit to indicate a cable break (HW class shows the value -2147483632)	
Input type	difference input	
Resolution	16-bit (ca. 0.3 mV / LSB)	
Conversion time for all channels	FW version V01.00: 15.26 µs FW version ≥ V02.00: depending on the selected timing Speed mode: 15.26 µs Time offset mode: corresponds to the S-DIAS cyclic time	
Common mode range	±12 V	
Input resistance	typically 660 kΩ	
Cable break monitor	yes	
Input filter hardware	typically 1 kHz, low pass 3rd order system	
Input filter software	configurable, low pass 1st order system	
Basic accuracy	±0.20 % of maximum measurement value	
Total accuracy (0-60 °C)	±0.30 % of maximum measurement value	

1.5 Analog Current Input Specifications

Number of channels	1	
Measurement range	0-20 mA	4-20 mA
Measurement value	0-20,000 or 0-60,000 (at Full-Range)	4,000-20,000 or 12,000-60,000 (at Full-Range)
		With an open input, the firmware returns the positive maximum value and a status bit to indicate a cable break (HW class shows the value -2147483632)
Input type	difference input	
Resolution	16-bit (ca. 0.3 µA/LSB)	
Conversion time for all channels	FW version V01.00: 15.26 µs FW version ≥ V02.00: depending on the selected timing Speed mode: 15.26 µs Time offset mode: corresponds to the S-DIAS cyclic time	
Common mode range	±10 V	
Input resistance	typically 50 Ω	
Cable break monitor	no	yes, settable via software between 0-4 mA (default: 3 mA)
Short-circuit monitor	no	yes, settable via software between 0-4 mA (default: 3 mA)
Input filter hardware	typically 1 kHz, low pass 3rd order	
Input filter software	configurable low pass 1st order system	
Basic accuracy	±0.30 % of maximum measurement value	
Total accuracy (0-60 °C)	±0.50 % of maximum measurement value	

1.6 Electrical Requirements

Power supply +24 V	18-30 V DC [1]	
Current consumption of the +24 V supply	corresponds to the load on the digital outputs	
Voltage supply from the S-DIAS bus	+5 V	
Current consumption on the S-DIAS bus (+5 V power supply)	typically 60 mA	maximum 65 mA
Voltage supply from the S-DIAS bus	+24 V	
Current consumption on the S-DIAS bus (+24 V power supply)	typically 20 mA	maximum 25 mA
UL standard	for UL[1] : must be supplied with SELV / PELV and Limited Energy	

[1] In U.S. according to Class 2 UL 508 intended to be supplied from a Class 2 transformer or power source in the field. Secondary circuit evaluated to the requirements of UL 508 section 63.29 in exception no. 1 of section 32.4.4 or 32.5.1. Isolating source and ratings of the overcurrent protective devices required to be installed with Limited Voltage / Current.

If this S-DIAS module is connected to an S-DIAS supply module with several S-DIAS modules, the total current of the modules used must be determined and checked.

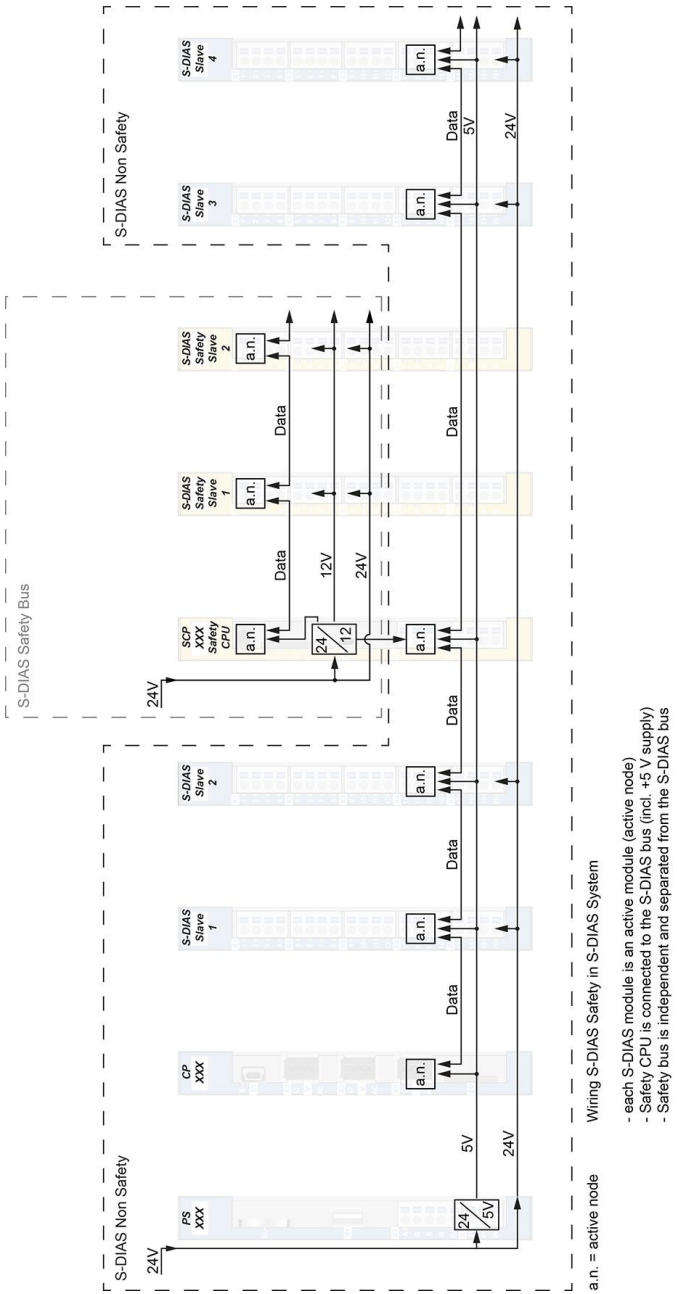
The total current of the +24 V supply cannot exceed 1.6 A!
The total current of the +5 V supply cannot exceed 1.6 A!

The specification for the current can be found in the module-specific technical documentation under "Electrical Requirements".

Si ce module S-DIAS est connecté à un module d'alimentation S-DIAS suivi de plusieurs modules S-DIAS, le courant total des modules utilisés doit être déterminé et vérifié.

Le courant total de l'alimentation +24 V ne peut pas dépasser 1,6 A!
Le courant total de l'alimentation +5 V ne peut pas dépasser 1,6 A!

Le cahier des charges pour le courant peut être trouvé dans la documentation spécifique au module sous "Spécifications électriques".


S-DIAS Non Safety
S-DIAS Safety Bus
S-DIAS Non Safety
24V
PS XXX
CP XXX
S-DIAS Slave 1
S-DIAS Slave 2
SCP XXX Safety CPU
S-DIAS Safety Slave 1
S-DIAS Safety Slave 2
S-DIAS Slave 3
S-DIAS Slave 4
a.n.
Data
5V
12V
24V
24/5V
24/12
a.n. = active node
Wiring S-DIAS Safety in S-DIAS System
- each S-DIAS module is an active module (active node)
- Safety CPU is connected to the S-DIAS bus (incl. +5 V supply)
- Safety bus is independent and separated from the S-DIAS bus

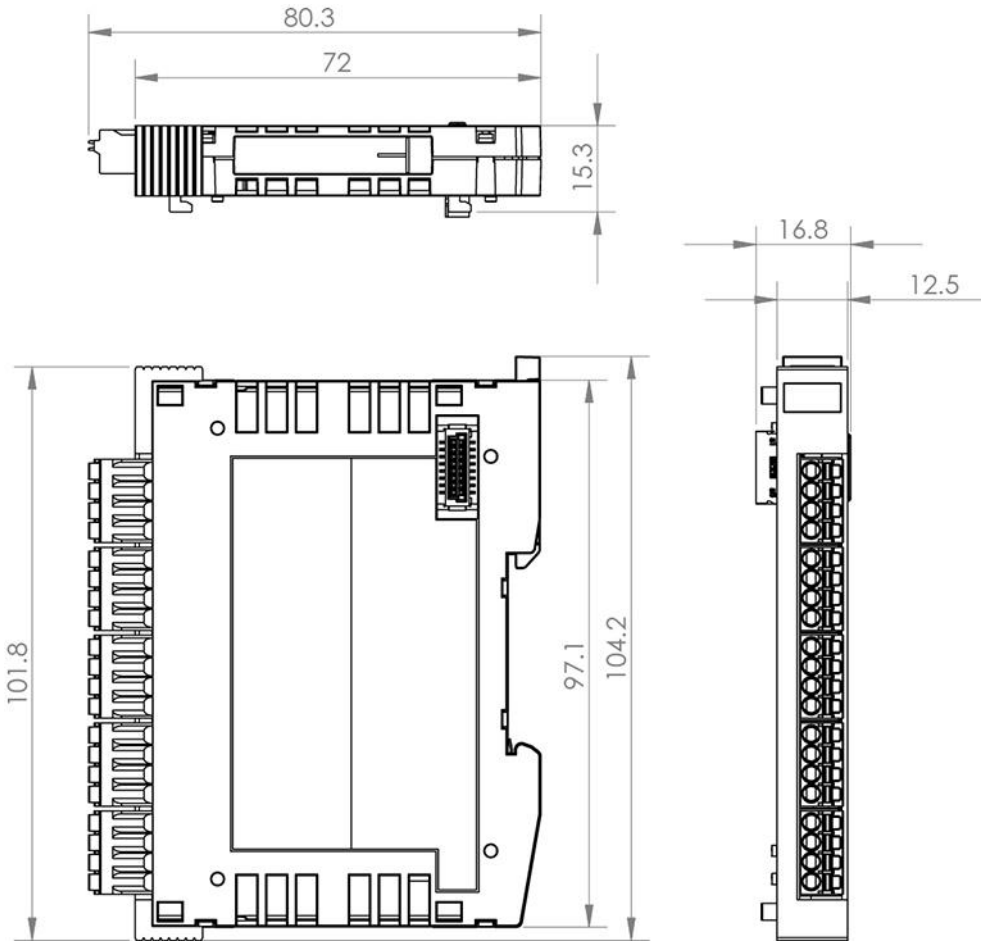
1.7 Miscellaneous

Article number	20-013-011
Hardware version	1.x
Standard	UL 508 (E247993)
Approbations	UL, cUL, CE

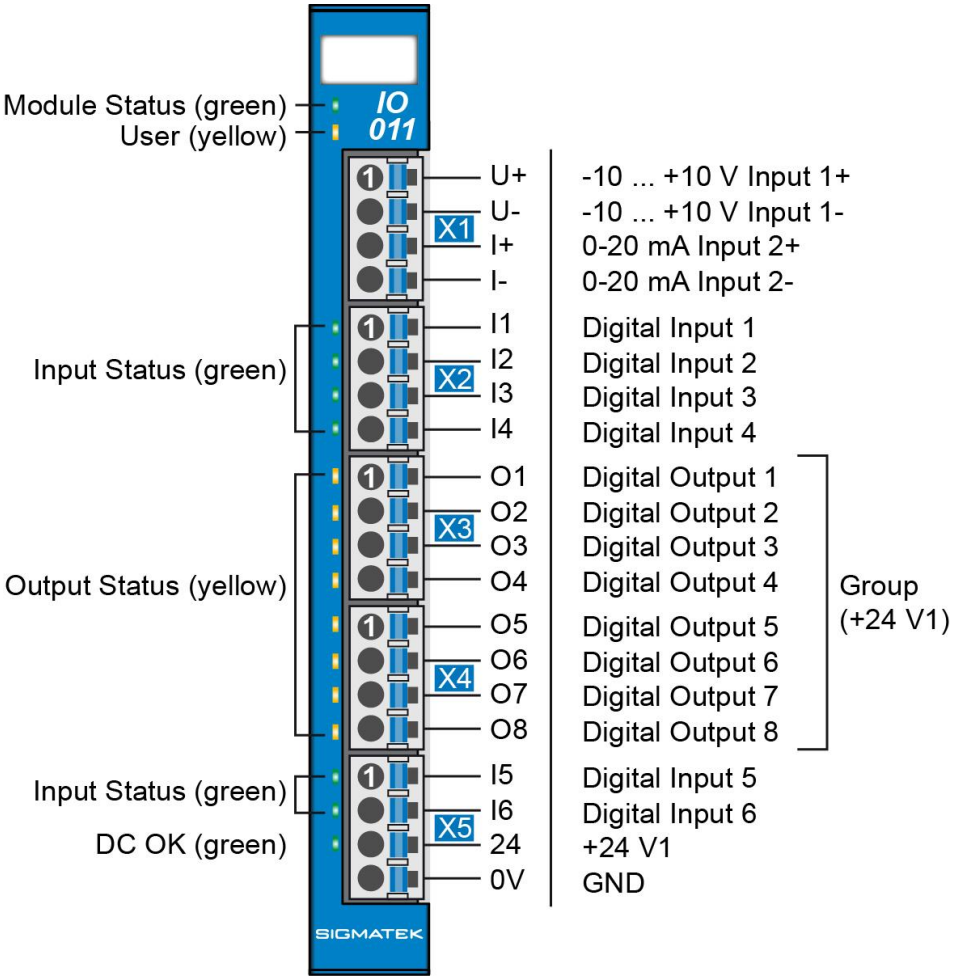
1.8 Environmental Conditions

Storage temperature	-20 ... +85 °C	
Environmental temperature	0 ... +60 °C	
Humidity	0-95 %, non-condensing	
Installation altitude above sea level	0-2000 m without derating > 2000 m with derating of the maximum environmental temperature by 0.5 °C per 100 m	
Operating conditions	Pollution degree 2 altitude up to 2000 m	
EMC resistance	in accordance with EN 61000-6-2:2007 (industrial area)	
EMC noise generation	in accordance with EN 61000-6-4 (industrial area)	
Vibration resistance	EN 60068-2-6	3.5 mm from 5-8.4 Hz 1 g from 8.4-150 Hz
Shock resistance	EN 60068-2-27	15 g
Protection type	EN 60529	IP20

2 Mechanical Dimensions



3 Connector Layout



3.1 Status LEDs

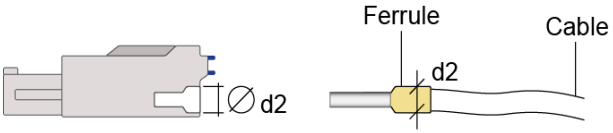
Module Status	green	ON	module active
		OFF	no supply available
		BLINKING (5 Hz)	no communication
User	yellow	ON	can be set from the application (e.g. the module LED can be set to blinking through the visualization so that the module is easily found in the control cabinet)
		OFF	
		BLINKING (2 Hz)	
		BLINKING (4 Hz)	
Input Status	green	ON	input on
		OFF	input off
Output Status	yellow	ON	output on
		OFF	output off
DC OK	green	ON	voltage is supplied to the output group

3.2 Applicable Connectors

Connectors:
X1-X5: Connectors with spring terminals (included in delivery)
The spring terminals are suitable connecting ultrasonically compacted (ultrasonically welded) strands.

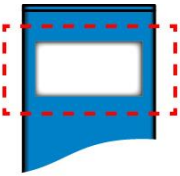
Connections:

Stripping length/Sleeve length:	10 mm
Mating direction:	parallel to the conductor axis or circuit board
Conductor cross section rigid:	0.2-1.5 mm^2
Conductor cross section flexible:	0.2-1.5 mm^2
Conductor cross section ultrasonically compacted:	0.2-1.5 mm^2
Conductor cross section AWG/kcmil:	24-16
Conductor cross section flexible with ferrule without plastic sleeve:	0.25-1.5 mm^2
Conductor cross section flexible with ferrule with plastic sleeve:	0.25-0.75 mm^2 (reason for reduction d2 of the ferrule)



d2 = max. 2.8 mm

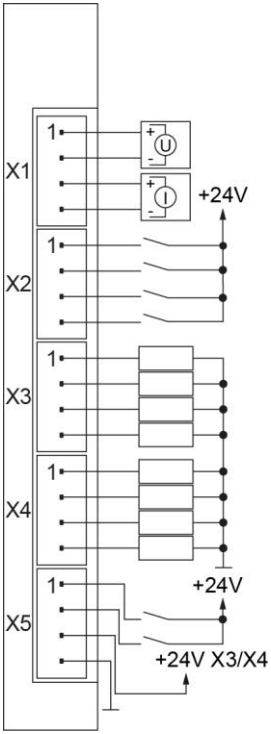
3.3 Label Field



Manufacturer	Weidmüller
Type	MF 10/5 CABUR MC NE WS
Weidmüller article number	1854510000
Compatible printer	Weidmüller
Type	Printjet Advanced 230V
Weidmüller article number	1324380000

4 Wiring

4.1 Wiring Example

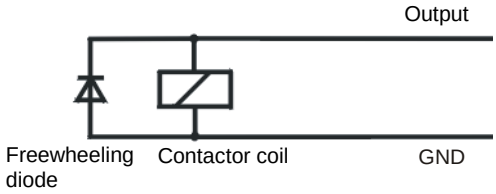


4.2 Notes Concerning Digital Outputs

- Up to 8 outputs are powered by a common +24 V supply.
- The cross section of the conductor for the +24 supply must be sufficient for the maximum total current.
- The outputs can be turned off by turning off the +24 V supply voltage.
- Applying power to an output whose supply voltage exceeds 0.7 V is not allowed.

Inductive loads must always be connected to a freewheeling diode or an RC network. This should be placed as close to the load as possible.

4.2.1 Connecting Inductive Loads



4.3 Notes Concerning Analog Inputs

The signals recorded by the analog modules are very small in comparison to the digital signals. To ensure error-free operation, a careful wiring method must be followed:

- The DIN rail must have an adequate mass connection.
- The lines connected to the source of the analog signals must be as short as possible and parallel wiring to digital signal lines must be avoided.
- The signal lines must be shielded.
- The shielding must be connected to a shielding bus.
- Avoid parallel connections between input lines and load-bearing circuits.
- Protective circuits for all relays (RC networks or free-wheeling diodes)

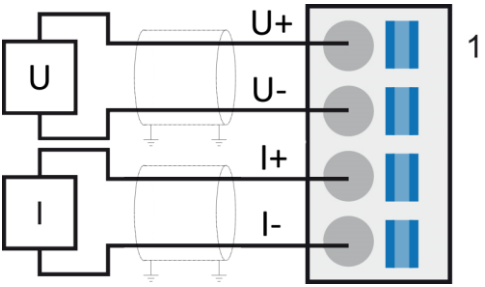
The ground bus should be connected to the control cabinet when possible!

Si possible la terre doit être connectée à l'armoire de commande!

IMPORTANT:
The S-DIAS module CANNOT be connected/disconnected while voltage is applied!

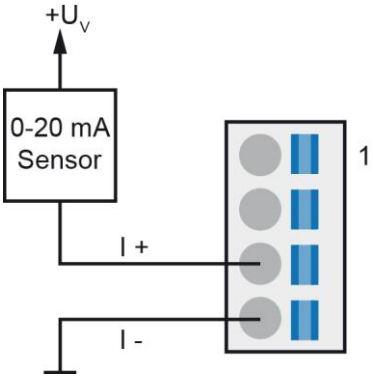
Le module S-DIAS ne peut pas être inséré ou retiré sous tension.

4.4 Connecting the Signal Source

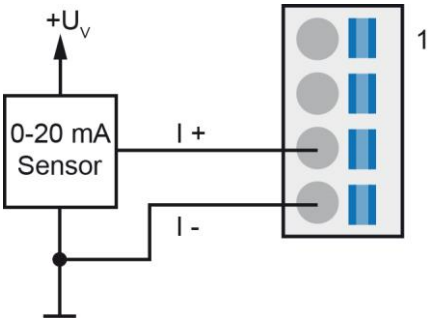


IMPORTANT:
The common mode range of ±10 V must be obtained for each signal pin.

4.5 Connection of a 2-wire Sensor

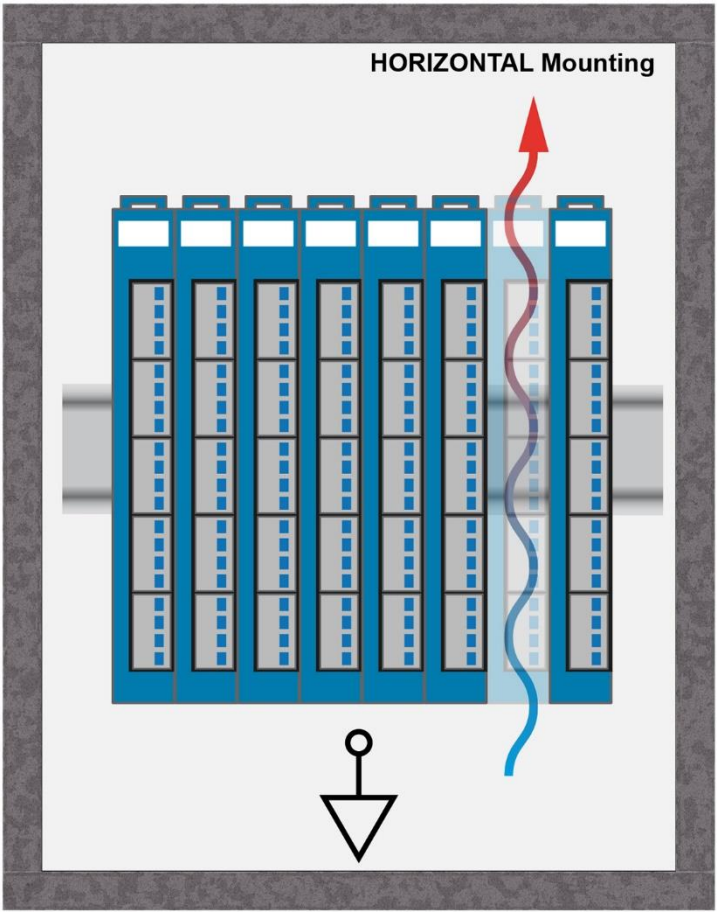


4.6 Connection of a 3-wire Sensor

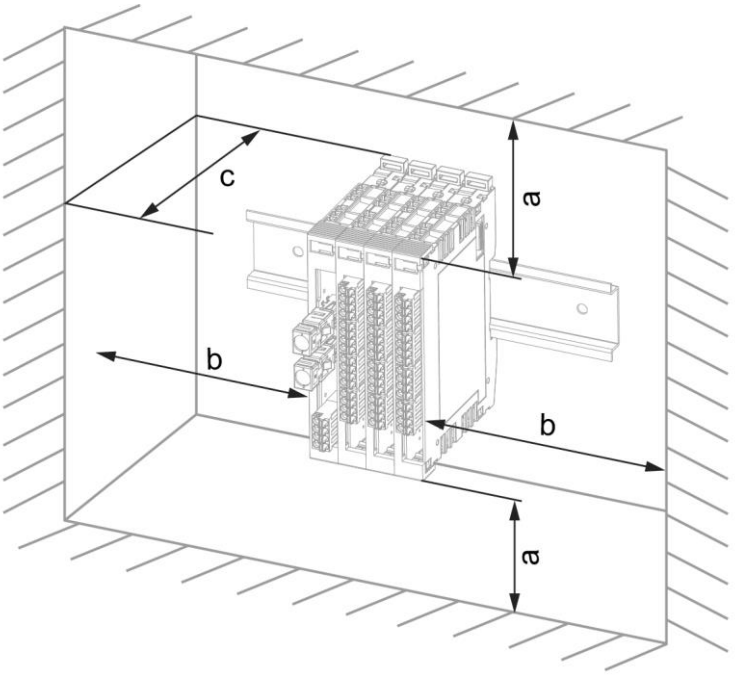


5 Mounting

The S-DIAS modules are designed for installation into the control cabinet. To mount the modules a DIN-rail is required. The DIN rail must establish a conductive connection with the back wall of the control cabinet. The individual S-DIAS modules are mounted on the DIN rail as a block and secured with latches. The functional ground connection from the module to the DIN rail is made via the grounding clamp on the back of the S-DIAS modules. The modules must be mounted horizontally (module label up) with sufficient clearance between the ventilation slots of the S-DIAS module blocks and nearby components and/or the control cabinet wall. This is necessary for optimal cooling and air circulation, so that proper function up to the maximum operating temperature is ensured.



Recommended minimum distances of the S-DIAS modules to the surrounding components or control cabinet wall:



a	b	c
30 mm (1.18˝)	**30 mm** (1.18˝)	**100 mm** (3.94˝)

a, b, c … distances in mm (inches)

6 Expanded Timing Mode (FW Version ≥ V02.00)

The IO 011 can be operated either in speed mode or in time-offset modus. This can be configured in the Info byte of the configuration data (address 0x0104).

6.1 Speed Mode

In this mode, the analog inputs are scanned as fast as possible and filtered to achieve the highest possible sampling rate. The timepoint of the individual measurements cannot be defined since measuring is continuous.

6.2 Time-Offset Mode

In the time-offset mode, the analog inputs are measured only once per cycle (the duration of a cycle corresponds to the S-DIAS cyclic time). This is then entered as an offset in µs from the cycle start point (S-DIAS Sync).

The settable values (time offsets) are subject to the following limits:

- **The time offset goes into effect in the following cycle:** The time offset values must be cyclically transferred from the hardware to the software. These however, only become effective in the next cycle since the firmware must first test and activate the values.

- **Minimum time offset value:** Since the firmware must process the incoming cyclic data immediately after the S-DIAS sync, only offset values of **105 µs** and higher can be used.

- **Maximum time offset value:** Since cyclic Data for the HW class must be sent at the end of an S-DIAS cycle, only offset values up a maximum cycle time **below 197 µs** can be used.

- **Interval between time offsets:** Since it is not possible to measure multiple analog inputs simultaneously, the interval between offsets must be at least **8 µs**.

- **Correction within the firmware:** If offset values are set beyond the limits or too close together, these are corrected (shifted) by the firmware where possible. To signal the correction or incorrect values to the HW class, the appropriate status bit is set (bit 6 of 7 in the cyclic data for the HW class at address 0x000A).

7 Addressing

7.1 FPGA – HW Class Addressing

Digital in and outputs are operated by the FPGA of the IO 011 directly. Whereby, a section of the address area is therefore required. This area is not used by the firmware.

Address (hex)	Size (bytes)	Access Type	Description
0000	**4**	**r**	**Data for the HW Class**
0000	4	r	Input register Bit 0-15 reserved Bit 16 digital input 1 Bit 17 digital input 2 Bit 18 digital input 3 Bit 19 digital input 4 Bit 20 digital input 5 Bit 21 digital input 6 Bit 22 DIAG back-reading Bit 23: DC 24V ok Bit 24 back-reading digital output 1 Bit 25 back-reading digital output 2 Bit 26 back-reading digital output 3 Bit 27 back-reading digital output 4 Bit 28 back-reading digital output 5 Bit 29 back-reading digital output 6 Bit 30 back-reading digital output 7 Bit 31 back-reading digital output 8
0000	**4**	**w**	**Data for FPGA**
0000	4	w	Output register Bit 0-23 reserved Bit 24 digital output 1 Bit 25 digital output 2 Bit 26 digital output 3 Bit 27 digital output 4 Bit 28 digital output 5 Bit 29 digital output 6 Bit 30 digital output 7 Bit 31 digital output 8

7.2 Firmware – HW Class Addressing (FW Version V01.00)

The address allocation defined here applies to the FW version V01.00.

Address (hex)	Size (bytes)	Access Type	Description
0080	**128**	**w**	**Cyclic Data for Firmware**
-	-	-	No cyclic data for firmware available
0004	**124**	**r**	**Cyclic Data for the HW class**
0004	2	r	Status Bit 0 24 V DC not OK Bit 1 not synchronized Bit 2 FLASH calibration data CRC error Bit 3 RAM calibration data CRC error Bit 4 invalid calibration data Bit 5 S-DIAS cyclic time not supported Bit 6-15 reserved
0006	2	r	Analog input 1 - voltage
0008	2	r	Analog input 2 - current
000A	1	r	Cable break detection Bit 0 cable break AI1 - voltage Bit 1 cable break AI2 - current Bit 2-4 reserved Module status Bit 5 AI2 over range (over current) Bit 6-7 reserved
000B	1	r	Reserved
0100	**128**	**w**	**Firmware Configuration Data**
0100	2	w	CRC16 over the entire configuration data
0102	2	w	Length of the configuration data

0104	1	w	Info (special-purpose or status bits) Bit 0 raw value mode 0 … normal mode (input values are calibrated) 1 ... raw values are provided Bit 1 boot loader/update request Bit 2-7 reserved
0105	1	w	Reserved
0106	1	w	Selection of the analog input measurement ranges Bit 0 analog input 1 - voltage 0 … -10 V to +10 V measurement range 1 ... 0 V to +10 V measurement range Bit 1 analog input 2 - current 0 … 0-20 mA measurement range 1 ... 4-20 mA measurement range Bit 2-7 reserved
0107	2	w	Frequency limit low pass filter in Hz analog input 1 - voltage (with a frequency limit setting of 0 Hz, the software low pass filter is deactivated. Compliance with the sampling theorem must be ensured)
0109	2	w	Frequency limit low pass filter in Hz analog input 2 - current (with a frequency limit setting of 0 Hz, the software low pass filter is deactivated. Compliance with the sampling theorem must be ensured)
010B	2	w	Value limit for cable break detection in AI2 (in µA from 0 - 4000, only active if the input is operated in the 4-20 mA measurement range)
010D	2	w	Message counter
010F	1	w	Reserved
0180	**128**	**r**	**HW Class Configuration Data**
0180	2	r	CRC16 over the entire configuration data
0182	2	r	Length of the configuration data
0184	2	r	Firmware version
0186	2	r	Message counter (copy of the received message counter to confirm acceptance of the configuration data)

7.3 Firmware – HW Class Addressing (FW Version ≥ V02.00)

The address allocation defined here applies to the FW version ≥ V02.00.

Address (hex)	Size (bytes)	Access Type	Description
0080	**128**	**w**	**Cyclic Data for Firmware**
0080	2	w	AI 1 – time-offset from Sync in µs (the time offsets are automatically adjusted, see 6.2)
0082	2	w	AI 2 – time-offset from Sync in µs (the time offsets are automatically adjusted, see 6.2)
0004	**124**	**r**	**cyclic Data for the HW class**
0004	2	r	Status Bit 0 24 V DC not OK Bit 1 not synchronized Bit 2 FLASH calibration data CRC error Bit 3 RAM calibration data CRC error Bit 4 invalid calibration data Bit 5 S-DIAS cyclic time not supported Bit 6-11 reserved Error information Bit 12-15 error codes 00 …….. no errors occurred 01 …….. periphery could not be initialized 02 …….. system clock could not be initialized 03-14 ..... reserved 15 …….. undefined error occurred
0006	2	r	Analog input 1 - voltage
0008	2	r	Analog input 2 - current

000A	1	r	Cable break detection and measurement range testing Bit 0 cable break AI1 - voltage (AI1 corresponds to an over range when the expanded measurement range test is activated) Bit 1 cable break AI2 - current (AI2 corresponds to an under range when the expanded measurement range test is activated) Bit 2-3 reserved Bit 4 (AI1 corresponds to an under range when the expanded measurement range test is activated) Bit 5 AI2 over range Time Offset Information Bit 6 time offset must be corrected (interval was too short or is beyond the limit) Bit 7 Time offsets exceed the allowed limits and cannot be corrected (the defined time offsets are invalid or became invalid by shifting the offsets within the firmware)
000B	1	r	Reserved
0100	**128**	**w**	**Firmware Configuration Data**
0100	2	w	CRC16 over the entire configuration data
0102	2	w	Length of the configuration data

0104	1	w	info (special-purpose or status bits) Bit 0 raw value mode 0 … Normal mode (input values are calibrated) 1 ... Raw values are provided Bit 1 boot loader/update request Bit 2 message counter offset 0 … message counter is expected at address 0x010D and is 2 bytes too large 1 … message counter is expected at address 0x0105 and is 2 bytes too large Bit 3 ADC - timing mode 0 … Speed mode (the ADC is read over a measurement timer as fast as possible) 1 … Time-offset mode (the analog inputs are sampled with the predefined time offsets of the HW class) Bit 4 full 16-bit resolution (full-range mode) 0 … full-range mode is disabled (the voltage values are provided in a range from -10000 mV to +10000 mV. The current values are provided in a range from 0 µA to 20000 µA) 1 … full-range mode is enabled (the resolution of the values is increased by a factor of 3, whereby the voltages are provided in a range from -30000 to +30000 units and currents in a range of 0 to 60000 units. the measurement range remains unchanged) Bit 5 expanded measurement testing 0 ... no additional measurement range testing. 1 … additional measurement range testing active (The incoming voltage values are tested for the measurement range and if the upper or lower limit is exceeded, the appropriate bits are set in the cyclic data. The incoming current values are tested in the 0-20 mA operating mode for under current (reverse polarity), the measurement range limit is ±1.25 % of the selected range. Bit 6-7 reserved
0105	1	w	Message counter (bit 2 in the info byte at address 0x0104 must be set, so that the message counter is used at this location)

0106	1	w	Selection of the analog input measurement range Bit 0 analog input 1 - voltage 0 … -10 V to +10 V measurement range 1 ... 0 V to +10 V measurement range Bit 1 analog input 2 - current 0 … 0-20 mA measurement range 1 ... 4-20 mA measurement range Bit 2-7 reserved
0107	2	w	Frequency limit low pass filter in Hz analog input 1 - voltage (with a frequency limit setting of 0 Hz, the software low pass filter is deactivated. Compliance with the sampling theorem must be ensured)
0109	2	w	Frequency limit low pass filter in Hz analog input 2 - current (with a frequency limit setting of 0 Hz, the software low pass filter is deactivated. Compliance with the sampling theorem must be ensured)
010B	2	w	Value limit for cable break detection in AI2 (in µA from 0 - 4000, only active if the input is operated in the 4-20 mA measurement range)
010D	2	w	Message counter (bit 2 in the info byte at address 0x0104 cannot be set, so that the message counter is used at this location)
010F	1	w	Reserved
0180	**128**	**r**	**HW Class Configuration Data**
0180	2	r	CRC16 over the entire configuration data
0182	2	r	Length of the configuration data
0184	2	r	Firmware version
0186	1	r	Message counter (copy of the received message counter to confirm acceptance of the configuration data)
0187	1	r	Reserved (if the message counter is 2 bytes too large (bit 2 in the info byte at address 0x0104 is set), this byte is then also required for the message counter)

8 Supported Cycle Times

8.1 Cycle Times below 1 ms (in µs)

FW	50	100	125	200	250	500
≥ V2.00						x

x= supported

8.2 Cycle Times equal to or above 1 ms (in ms)

FW	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
≥ V2.00	x	x		x				x								x

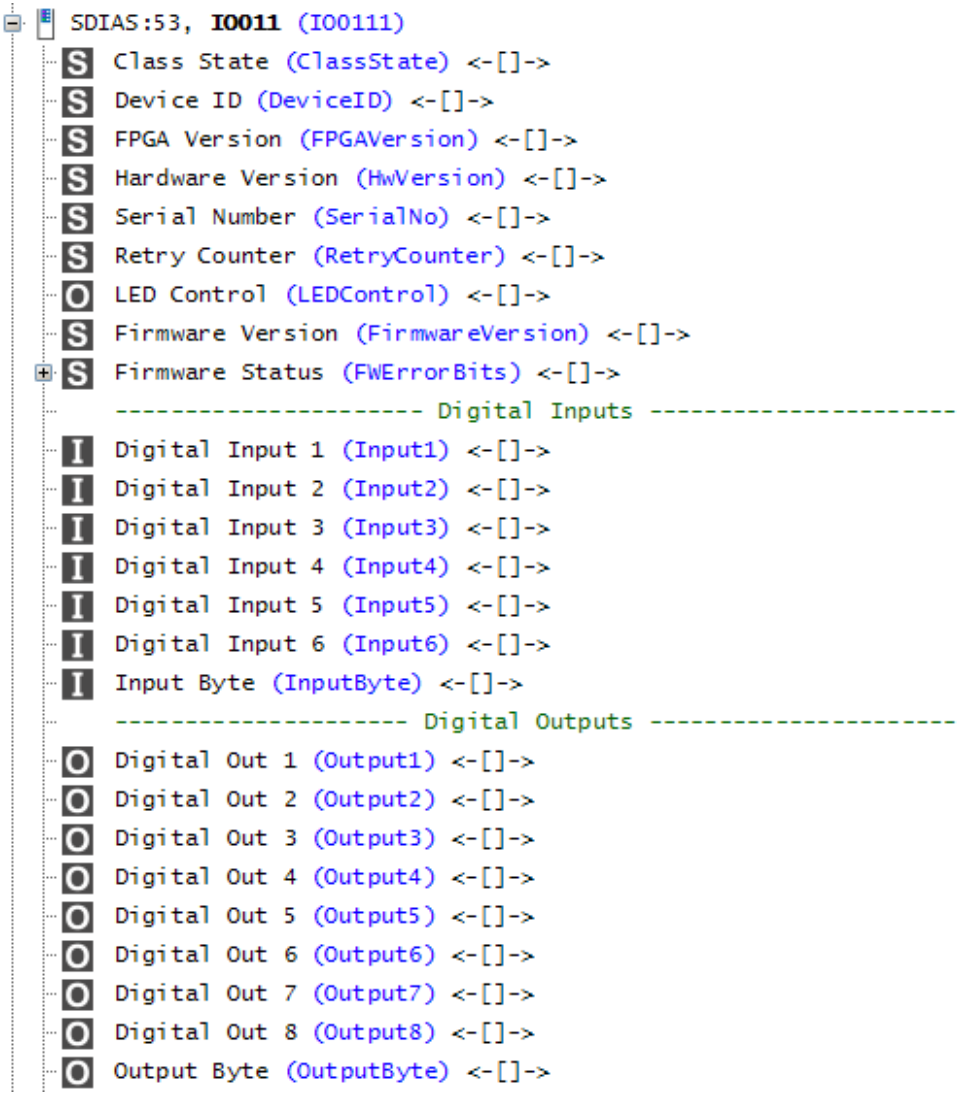
x= supported

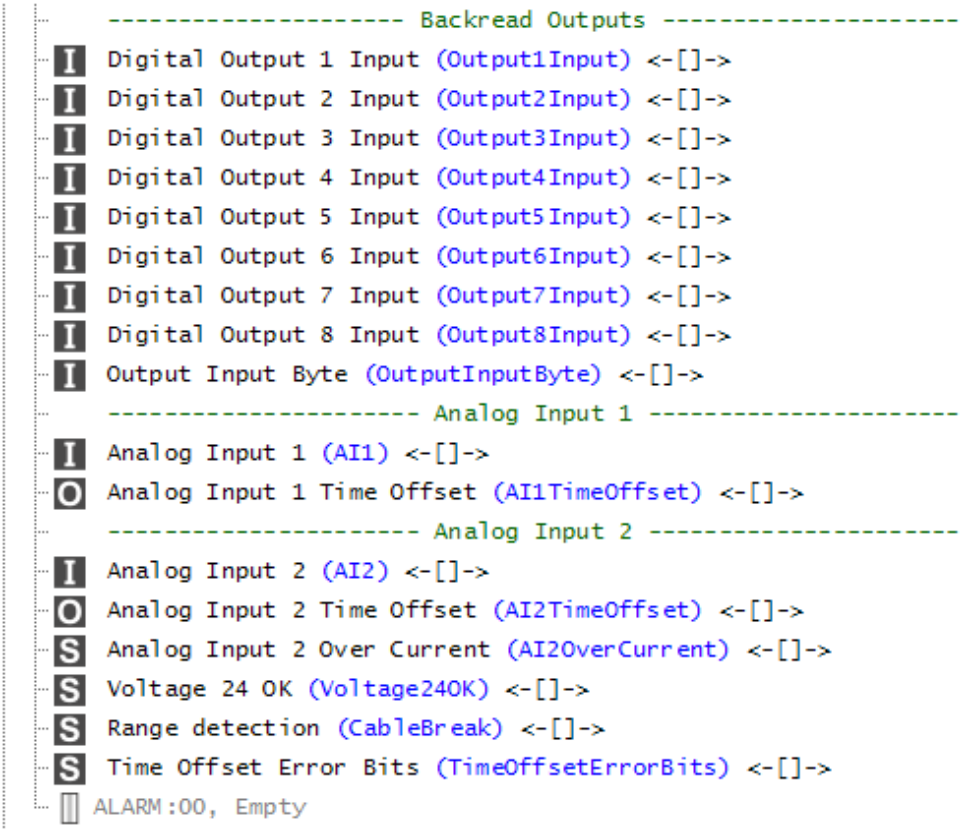
FW	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
≥ V2.00																x

x= supported

9 Hardware Class IO011

Hardware Class IO011 for the S-DIAS IO011 multi I/O module





This hardware class is used to control the IO 011 hardware module. The module has 6 digital inputs and 8 digital outputs (backreadable). Additionally 2 analog inputs are available.
More information on the hardware can be found in the module documentation.

9.1 General

Class State	State	This server shows the actual status of the hardware class.
Device ID	State	The device ID of the hardware module is shown in this server.
FPGA Version	State	FPGA version of the module in 16#XY (e.g. 16#10 = version 1.0).
Hardware Version	State	Hardware version of the module in format 16#XXYY (e.g. 16#0120 = Version 1.20)
Serial Number	State	The serial number of the hardware module is shown in this server.
Retry Counter	State	This server increments when a transfer fails.
LED Control	Output	With this server, the application LED of the S-DIAS module can be activated to find the module in the network more quickly. The following statuses are possible: 0 LED off 1 LED on 2 blinks slowly 3 blinks rapidly
Firmware version	State	The firmware version of the hardware module is shown in this server.
Firmware Status	State	In this server, the status bits of the FW are shown. The respective bits mean the following: Bit 0 DC not OK Bit 1 no Sync available Bit 2 Flash Data CRC Error Bit 3 Ram Data CRC Error Bit 4 invalid EEProm version Bit 5 bus cycle time not supported Bit 6 configuration invalid
Required	Property	This client is active by default, which means that the S-DIAS hardware module at this position is mandatory for the system and can under no circumstances be disconnected or return an error. Otherwise, the entire hardware deactivated. If the hardware module is missing or removed, an S-DIAS error is triggered. If his client is initialized with 0, the hardware module located in this position is not mandatory. This means that it can be inserted or removed at any time. However, which components identified as "not required" should be selected with regard to the safety of the system.

9.2 Digital Inputs and Outputs

Input [1-6]	Input	Shows the status of the digital input [1-6].
Output [1-8]	Output	With this server the digital output [1-8] can be controlled. Sets output via the write method of the server.
Output [1-8] Input	Input	Shows the backreadable status of the digital outputs [1-8].
Input Byte	Input	In this server, the digital outputs are shown in an 8-bit field. Within it bit 0 to bit 5 are assigned to the inputs Input1 to Input6.
Output Byte	Output	In this server, the digital outputs are shown in a 8-bit field. Within it bit 0 to bit 7 are assigned to the outputs Output1 to Output8. A write() instruction to this server writes the bit pattern to these outputs.

9.3 Analog Inputs

AI1 Config	Property	0 AI1 used as analog input (Range: -10 V to +10 V) 1 AI1 used as analog input (Range: 0 V to +10 V)
AI2 Config	Property	0 AI2 used as analog input (Range: -10 V to +10 V) 1 AI2 used as analog input (Range: 0 V to +10 V)
AI[1-2] cut off frequency	Property	In this client, the cutoff frequency for the software low pass filter is set. Value setting options are: 0 1000 Hz 1 500 Hz 2 250 Hz 3 100 Hz 4 50 Hz 5 25 Hz 6 10 Hz
AI[1-2] minimal value	Property	This value indicates the minimum value for the channel. If on the channel the minimum value (depending on AI[1-2]Config) is measured, then in the software this value is output. With the settings on the clients AI[1-2]_Min and AI[1-2]_Max the range of the measurement values is defined.
AI[1-2] maximal value	Property	This value indicates the maximum value for the channel. If on the channel the maximum value (depending on AI[1-2]Config) is measured, then in the software this value is output. With the settings on the clients AI[1-2]_Min and AI[1-2]_Max the range of the measurement values is defined.
Analog Input [1-2]	Input	Analog input 1-2, status query over read().

Cable Break	State	Cable break detection of the analog inputs: Bit 1: upper measurement range violated at input AI1 (cable break) Bit 2: lower measurement range violated at input AI2 (cable break) Bit 5: lower measurement range violated at input AI1 (is supported with FW version 2.00 or higher) Bit 6: upper measurement range violated at input AI2
Cable Break Limit	Property	Configurable limit for the detection of the lower measurement limit (cable break detection). Value range 0-4000 [µA]. (3000 default value = 3 mA) Valid with using firmware version >= 1.10. With firmware versions < 1.10 the value is < 3,75 mA As initialization value
Reference Voltage OK	State	Shows if the reference voltage is OK. 0: OK 1: not OK
Analog Input 2 Over Current	State	Shows if the current at the channel 2 is too high. 0: OK 1: not OK
Full Resolution 16 Bit	Property	Is used to activate the 16-bit resolution. This function is available since firmware version 2.00. 0: resolution voltage: -10/+10 V 1 mV LSB resolution current: 0 .. 20 mA 1 µA LSB (real 16 bit resolution) (FW Version 2.00 or higher) 1: resolution voltage: -10/+10 V 0.3 mV LSB resolution current: 0 .. 20 mA 0.3µA LSB As initialization value

9.4 Communication Interfaces

ALARM	Downlink	With this downlink the corresponding alarm class can be placed via the hardware editor.

9.5 Time Offset Mode

available since firmware version ≥ 2.00

Activate Time Offset Analog In	Property	This setting defines, whether the time offset mode for the analog inputs should be used. 0 Time offset mode for analog inputs deactivated 1 Time offset mode for analog inputs activated If 1 is set and the firmware of the module does not support this mode, the Class State is set to _ClientNotReady and a log message is output. As initialization value
Analog Input [1-2] Time Offset	Output	Time offset for the according analog input in µs. Valid limits: 105 µs to (cycle time - 197 µs). Example: 1 ms cycle time (bus time) ... Range: 105 µs to 803 µs Input value/status value: -1 Feature is not supported by the current firmware. (Available for FW version ≥ 2.00 or higher) -2 Defined value is outside the valid limits
Time Offset Error Bits	State	Bit 1 The defined time offsets were invalid and have automatically been adjusted by the firmware. This can happen, if the difference between two time offsets is too small (lower than 20 µs). Bit 2 The defined time offsets were invalid and could not be adjusted automatically by the firmware. This can happen, if the time offsets are defined too narrow, e.g. several time offsets are exactly at 105 µs before the sync.

9.5.1 Time Offset Mode for Analog Inputs

This mode allows to define the conversion time for each single analog input channel in µs in relation to the SDIAS sync during runtime. For this, the according value must be written to one of the servers “AI[x]TimeOffset”. This is accepted by the firmware with the next SDIAS sync.

9.5.2 Limitations of this Mode

- The configuration of new time offsets is not accepted by the firmware before the next cycle.
- Offsets are only valid 105 µs after the sync. All lower inputs are not accepted by the hardware class.
- Offsets are only valid up to 197 µs before the sync. All higher inputs are not accepted by the hardware class.
- The difference between two time offsets must be at least 20 µs. All other inputs are moved into the according range by the firmware. Then, the according status bit is set.

Documentation Changes

Change date	Affected page(s)	Chapter	Note
30.01.2017	1		"Differential" in the description of the inputs removed
30.06.2017	5, 6	1.4 ±10 V Analog Input Specifications 1.5 Analog Current Input Specifications	Document adapted to FW version V02.00
	19	6 Expanded Timing Mode (FW version V02.00)	Chapter added
	20-26	7 Addressing	Expansion:
19.07.2017	5	1.4 ±10 V Analog Input Specifications	Conversion time for all channels
	6	1.5 Analog Current Input Specifications	
17.08.2017	9	1.8 Environmental Conditions	Added operating conditions
	12	3.2 Applicable Connectors	Added sleeve length Added info regarding ultrasonically welded strands
18.10.2017	13	3.3 Label Field	Added chapter
	19	5 Mounting	Graphic replaced
03.11.2017	18	4.5 Connection of a 2-wire Sensor 4.6 Connection of a 3-wire Sensor	Chapter added
22.11.2017	7	1.6 Electrical Requirements	Added UL standard and explaining footnote
03.05.2018	5, 6	1.4 ±10 V Analog Input Specifications 1.5 Analog Current Input Specifications	Common mode range, Basic accuracy, Total accuracy Cable break monitor, Short-circuit monitor, Basic accuracy, Total accuracy
18.07.2019	29	8 Supported Cycle Times	Chapter added
13.08.2020	5, 6, 21, 25, 29	Whole document	FW version V02.00 adapted to FW version ≥ V02.00. Under chapter 8 x=supported added
08.09.2020	30	9 Hardware Class IO011	Chapter added
04.11.2020	19	5 Mounting	Expansion functional ground connection

03.09.2021	4	1.1 Digital Input Specifications	Signal level and Switching threshold